IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)
	)
QING MA	)
QUAN TRAN	)
STEVE TOWLE	)
EBRAHIM ANDIDEH	)
	) Examiner: D. Le
Serial No.: 10/038,343	)
	) Art Unit: 2818
Filed: January 2, 2002	)
	) Attorney Docket: 042390.P8125D
For: A SEMICONDUCTOR DEVICE HAVING A LOW-K DIELECTRIC LAYER	)
Which is a Divisional of Application:	)
	) Examiner: D. Le
Serial No.: 09/524,766	)
	) Art Unit: 2818
Filed: March 14, 2000	)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF QING MA UNDER 37 C.F.R. § 1.131

Dear Sir:

I, Qing Ma, declare that:

1. I am an inventor of the subject matter claimed in the captioned non-provisional patent application.

2. No later than October 4, 1999, I and my co-inventors generated an invention disclosure that described a multilayer laminate for use in a semiconductor device. The invention disclosure illustrated a two layer laminate that included a carbon doped oxide layer and a tougher film that was under compressive stress such as silicon dioxide or silicon nitride,

and illustrated a four layer laminate that included a first carbon doped oxide layer, a first thin coating of the tougher film, a second carbon doped oxide layer, and a second thin coating of the tougher film. Attached as Exhibit A is a true and correct copy of that invention disclosure dated October 4, 1999, as shown on page 3 of the exhibit.

3. Soon after submitting the invention disclosure to the Intel Corporation legal department, no later than November 1999, I was informed that a patent application would be filed for the invention that is described in Exhibit A.

4. After receiving and reviewing a draft patent application that accurately and completely described my invention, I signed a Declaration and Power of Attorney form and an assignment for the patent application, which were sent to Mark V. Seeley, the patent attorney who drafted the patent application.

5. I understand that this declaration is being submitted to support a response to an Office Action mailed on October 21, 2004 for U.S. Patent Application Serial Number 10/038,343 entitled "A Semiconductor Device Having a Low-K Dielectric Layer."

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the captioned application or any patent issued thereon.

Date: 12/7/04

Qing Ma

INTEL CONFIDENTIAL

P8125

TMG/Process/Comm / TMG/CR

TMG INVENTION DISCLOSURE, Rev 1, 2/98
Located at: http://legal.intel.com

LEGAL ID# 13080 (legal dept. use only) DATE: NOV 10 1999

It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to **Janice Boulden, Intel Legal Department at JF3-147. You can submit electronically if all of the information is electronic, including drawings and supervisor approval.** If you have any questions regarding this form or to whom it should be forwarded, please call **503-264-0444**.

Fill out the below and follow the instructions:

RECEIVED
NOV 15 1999
PATENT DATABASE GROUP
INTEL LEGAL TEAM

1. **Field of the Invention:**
   - [X] Semiconductor Process: device and integration
   - [ ] Semiconductor Process + Equipment: thin films
   - [ ] Semiconductor Process + Equipment: etch/litho
   - [ ] Circuit Design
   - [ ] Flash
   - [ ] Test
   - [ ] CQN (Q&R)
   - [ ] Packaging
   - [ ] Boards/Cartridge
   - [ ] Automation
   - [ ] Other

Computer IP Coordinator
Sherry Wheeler SC1-02
2267

2. **Concise Title of Invention:**

Crack resistant low-k laminate structures

3. **Brief Description of Invention (please use only space provided and font #10 or larger. Write the Key Elements of the Invention):**

The invention is:

Laminates consisting of brittle low-k layers (e.g., carbon doped oxides) and SiO2 with compressive stress can significantly improve crack resistance.

Carbon doped oxide (CDO) materials have been considered as an important low-k candidate because of various attractive film properties and they can be deposited in PECVD equipment, similar to traditional oxide films. However, these CDO films can suffer severely from cracking, flaking, and delamination, making them challenging to integrate. A method to improve their crack resistance is to make a laminate structure of CDO and a material with higher toughness, keeping the second material thin so it will not significantly increase the k-value of the whole structure.

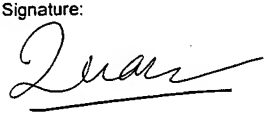
The key elements are:

A. Crack resistance of a brittle low-k material can be significantly improved by laminating the material with a tougher film with compressive stress (such as SiO2 and SiN).

4. Inventor(s):

Name:
Quan Tran
Phone:
(408) 765-2341
Citizenship:
USA
Group Name: TMG
Division Name: ATD___
PTD___ CTM___ CR_X__
STTD___ CQN ___
SMTD___TCAD___
Other?_____

SS# 612-52-4736 | Empl.# 10581923 | M/S: SC1-03
Fax: (408) 765-2949 | Home Address: 2048 Flintbury Ct. San Jose, CA 95148
Supervisor Name: Qing Ma | Supervisor Phone: 408-765-2116 | Supervisor M/S: SC1-03
BUM Presenter: John Carruthers | Inventor Signature:

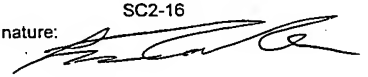


Name:
Qing Ma
Phone:
408-765-2116
Citizenship:
P.R. China
Group Name: TMG
Division Name: ATD___
PTD___ CTM___ CR_X__
STTD___ CQN ___
SMTD___TCAD___
Other?_____

SS# 191-64-5381 | Empl.# 10071627 | M/S: SC1-02
Fax: 408-765-2949 | Home Address: 919 Brentwood Dr., San Jose, CA 95129
Supervisor Name: Harry Fujimoto | Supervisor Phone: 408-765-2369 | Supervisor M/S: SC1-03
BUM Presenter: John Carruthers | Inventor Signature:

Name:
Steve Towle
Phone:
408-765-6464
Citizenship:
USA
Group Name: TMG
Division Name: ATD___
PTD___ CTM___ CR__
STTD___ CQN ___
SMTD___TCAD___
Other?___TME_____

SS# 004-68-8725 | Empl.# 10523564 | M/S: SC2-16
Fax: 408-765-2162 | Home Address: 206 S. Bayview Ave. Sunnyvale CA 94086
Supervisor Name: Steve Burke | Supervisor Phone: 765-2161 | Supervisor M/S: SC2-16
BUM Presenter: A.M. Kenitzer | Inventor Signature:



Name:

SS# | Empl.# | M/S:

Phone:

Fax: | Home Address:

Citizenship:

Supervisor Name: | Supervisor Phone: | Supervisor M/S:

Group Name: TMG
Division Name: ATD___
PTD___ CTM___ CR___
STTD___ CQN ___
SMTD___TCAD___
Other?_____

BUM Presenter: | Inventor Signature:

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

5. *HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (use first inventor's supervisor if multiple inventors)*

THOMAS M ARTEB FOR HARRY FUJIMOTO

DATE: 10/4/1999 SUPERVISOR NAME: Harry Fujimoto

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

6. **Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel?**
If yes, explain and give date:
(Give expected tape out date if applicable): No

7. **Has the subject matter of present disclosure been published or will it be published outside of Intel?**
If yes, explain and give date: No

8. **Has a product using or manufactured using the present disclosure been sold or offered for sale?**
If yes, explain and give date: No

9. **Has this invention been conceived, or constructed during accomplishment of a government or third party contract? If yes, give contract name and number: No**

10. **Explain the problem being addressed by the invention:**

This invention addresses the problem of:

Cracking of low-k films.

11. **Explain current state of the art (i.e, how the problem is solved today):**

Presently the problem described above is solved by:

Brittle low-k films are restricted to thicknesses well below their cracking threshold, often < 1um.

12. **Explain technical advantages of the invention over current state of the art:**

The technical advantages of this invention are:

1. It will enhance the mechanical integrity of low-k films, preventing films from cracking failure.

13. a. Is the invention experimentally verified? Yes
    b. Is the invention verified with simulation?
    c. If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis to justify that your invention will work (use extra space if necessary):

1. It was experimentally verified. Critical stress needed to crack film improved by 50% (from 80MPa to 120MPa). See attached memo.
2. The processing technology is standard. Invention could be implemented with a multistep reaction in a PECVD deposition chamber.
3. It has only a few percent impact on k.

14. Detailed Description of Invention (try to use only the space provided with font #10 or larger type. Refer to your drawings):

1. Figure 1a shows a brittle low-K film, such as CDO.
2. Figure 1b shows a double layer laminate that has a thin coating on low-k film. The thin coating has larger toughness and is under compressive stress (typical SiO2 and SiN)
3. Figure 1c shows a 4 layer laminate, which further improves crack resistance.

Referenced sketches/dwg's/diagrams: (use additional page(s))

15.

Drawings (use as many pages as needed)
(PLEASE DO NOT MAKE COLOR DRAWINGS)

Please see attached figures.

16. Key Supporting Data (1 page limit on separate page):

    Please see attached memo.

17. What is the product or process invention to be used on? (e.g., P8xx, name of product, etc.):

    P860 and beyond.

18. Have you reviewed your invention with a TMG Patent Mentor? (see below for mentor names) If so, give name: _____Yes. Chien Chiang_____

19. Any other information IP committee should consider?

MENTOR REVIEW

If you don't already have a departmental peer review process for invention disclosures, we recommend you have it reviewed by a Mentor before you send your invention disclosure to Intel Legal. The purpose of this Mentor review is to ensure that the invention disclosure is written clearly enough for the IP Committee to comprehend your invention including all the novel aspects of it. Please refer to the list below for recommended Mentors by area. Select ONE Mentor to review and acknowledge. This recommended step is not meant to unreasonably slow down the invention disclosure process. If your Mentor fails to respond to you in a reasonable amount of time, then send your invention disclosure directly to Intel Legal.

Area	Mentor
Semiconductor Process – device and integration	Mark Bohr, Robert Chau, Krishna Seshan, Greg Atwood
Semiconductor Process – thin films	Ken Cadien, Chien Chiang, John Carruthers
Semiconductor Process – etch/litho	John Carruthers, Peter Silverman, Peter Charvat (etch), Yan Borodovsky (litho)
Circuit Design	Ian Young, Greg Taylor, Clair Webb, Rajesh Galivanche, Greg Atwood
Flash	Greg Atwood, Krishna Seshan
Test	Wayne Needham, Rajesh Galivanche
CQN (Q&R)	Ian Young, Greg Taylor, Clair Webb, John Carruthers, Wayne Needham, Naomi Obinata
Packaging	Ken Kinsman, Jack McMahon
Boards/Cartridge	Leslie Polaski
Automation	Sanjay Natarajan
Other	Ray Werner, Naomi Obinata

Figure 1

a. A brittle low-K film, such as CDO.
b. A double layer laminate that has a thin coating on low-k film. The thin coating has larger toughness and is under compressive stress (typical SiO2 and SiN)
c. A 4 layer laminate, which further improves crack resistance.